INT21390

M O A B

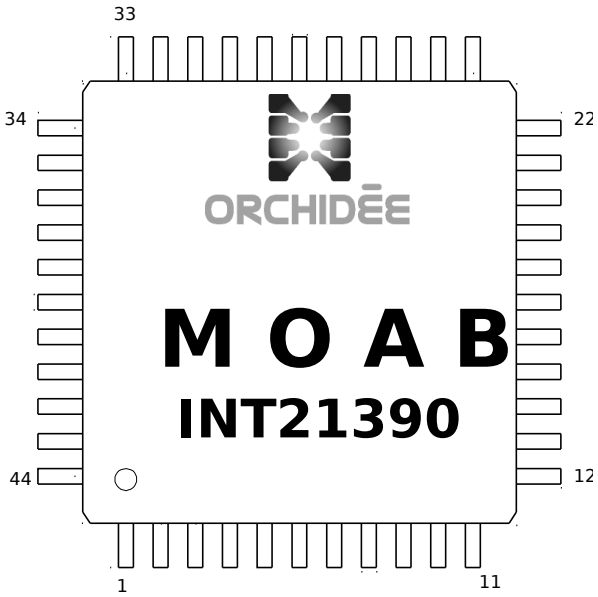
Orchidée Semiconductor 3.3V U_{pn} Terminal Line Transceiver

Features

- Pin-for-Pin replacement for industry-standard PSB21391 (SCOUT-P™) component without the CODEC
- Up to 3.0km (0.5mm) line interface performance (no dead zones)
- TE and TR (Terminal Repeater) mode support
- External Parallel Bus Interface (EPBI)
- HDLC with 64-byte receive and transmit FIFO's
- Low Power dynamic operation
- Single 3.3V supply
- 44-pin JDEC standard MQFP (Pb-free, green) package

Description

The Orchidée Semiconductor INT21390 is a fully featured replacement for the industry standard SCOUT-P™ without the CODEC. In place of the SCOUT-P™ CODEC pins the INT21390 includes and External Parallel (asynchronous) Bus Interface (EBPI). The EPBI operation is in lieu of the Monitor Channel Programming feature included on the SCOUT-P™. The chip supports loop lengths up to 3.0km over 0.5mm cable and provides all signal conditioning, equalization and adaptive threshold adjustment to optimize line performance. Most other features of the SCOUT-P™ are supported as well as several new features which are not supported in the SCOUT-P™.



SCOUT-P is a registered trademark of Infineon Technologies AG

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ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (V_{SS} = 0V, T_J = 25^{0}C)

Parameter	Symbol	Rated Values	Unit
Power Supply Voltage	V_{DD}	-0.3 to +7.0	V
Input Voltage	V_I	-0.3 to +7.0	
Output Voltage	V_O	-0.3 to VDD	
Input Current	I_I	-10 to +10	mA
Output Current per I/O	I_O	-10 to +10	
Storage Temperature	T_{STG}	-65 to +150	^{0}C

Recommended Operating Conditions (V_{SS} = 0V)

Parameter	Symbol	Rated Values	Unit
Power Supply Voltage	V_{DD}	+3.15 to +3.45	V
Junction Temperature	T_J	-40 to +100	^{0}C

DC Characteristics (Over Operating Range)

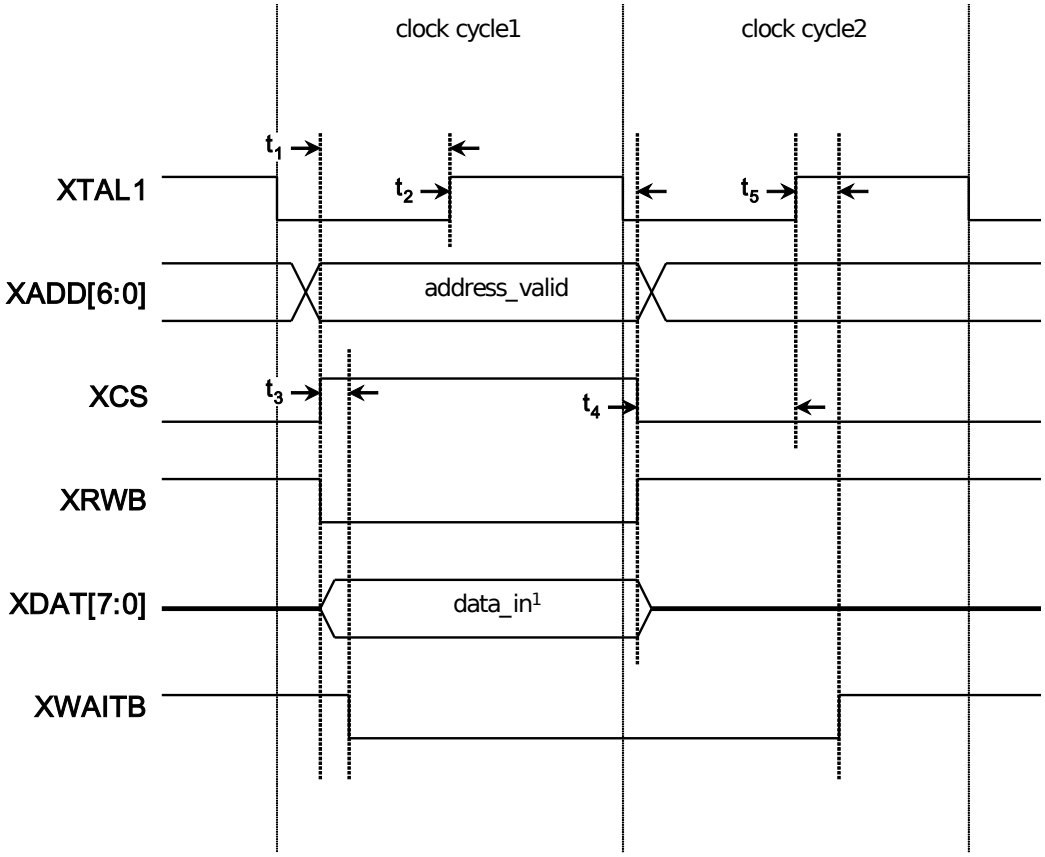
Parameter	Symbol	Conditions	Rated Values			Unit
			Min.	Typ.	Max.	
High Level Input Voltage	V_{IH}		2.0	-	V_{DD}	V
Low Level Input Voltage	V_{IL}		0.0	-	0.8	
High Level Output Voltage	V_{OH}	I_{OH} = TBD	2.4	-	-	
Low Level Output Voltage	V_{OL}	I_{OL} = TBD	-	-	0.4	
High Level Input Current	I_I	$V_{IH} = V_{DD}$	-	-	10	uA
Low Level Input Current	I_O	$V_{IL} = V_{SS}$	-10	-	-	
3-State Output Leakage Current	I_{OZH}		-10	-	10	
	I_{OZL}		-10	-	10	
Stand-by Current	I_{DDQ}	$V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$		TBD		

Pin Descriptions

Pin	Signal	Type	Description
1	XDAT[2]	I/O	EPBI data bus
2	XDAT[3]	I/O	EPBI data bus
3	XDAT[4]	I/O	EPBI data bus
4	XDAT[5]	I/O	EPBI data bus
5	XDAT[6]	I/O	EPBI data bus
6	XDAT[7]	I/O	EPBI data bus
7	CSB	Input	Active low chip select
8	INTB	Output	Open drain interrupt output signal
9	RSTB	Input	Asynchronous reset input
10	RSTO/SDS2	Output	Active low reset output, SDS2
11	SDS1	Output	SDS1
12	MCLK	Output	Output clock
13	XTAL2	Output	Output crystal clock
14	XTAL1	Input	Input clock
15	MODE	Input	0=TR mode, 1=TE mode
16	VDD	Supply	
17	VSS	Supply	
18	SCLK	Input	SCI clock
19	SDR	Input	SCI receive signal
20	SDX	Output	SCI open drain transmit signal
21	DD	I/O	IOM2 open drain data downstream
22	DU	I/O	IOM2 open drain data upstream
23	BCL	Output	IOM2 Bit clock output
24	DCL	I/O	IOM2 Data output clock
25	FSC	I/O	IOM2 Frame sync signal
26	XWAITB	Output	EPBI wait signal during bus access
27	XCS	Input	EPBI chip select input
28	XRWB	Input	EPBI active low write signal
29	XADD[0]	Input	EPBI address bus
30	VSS	Supply	
31	VDD	Supply	
32	LIA	Analog	Line interface
33	LIB	Analog	Line interface
34	XADD[1]	Input	EPBI address bus
35	VDDDETB	Input	Active low VDD detection enable
36	VDD	Supply	
37	VSS	Supply	
38	XADD[2]	Input	EPBI address bus
39	XADD[3]	Input	EPBI address bus
40	XADD[4]	Input	EPBI address bus
41	XADD[5]	Input	EPBI address bus
42	XADD[6]	Input	EPBI address bus
43	XDAT[0]	I/O	EPBI data bus
44	XDAT[1]	I/O	EPBI data bus

External Bus Interface Timing

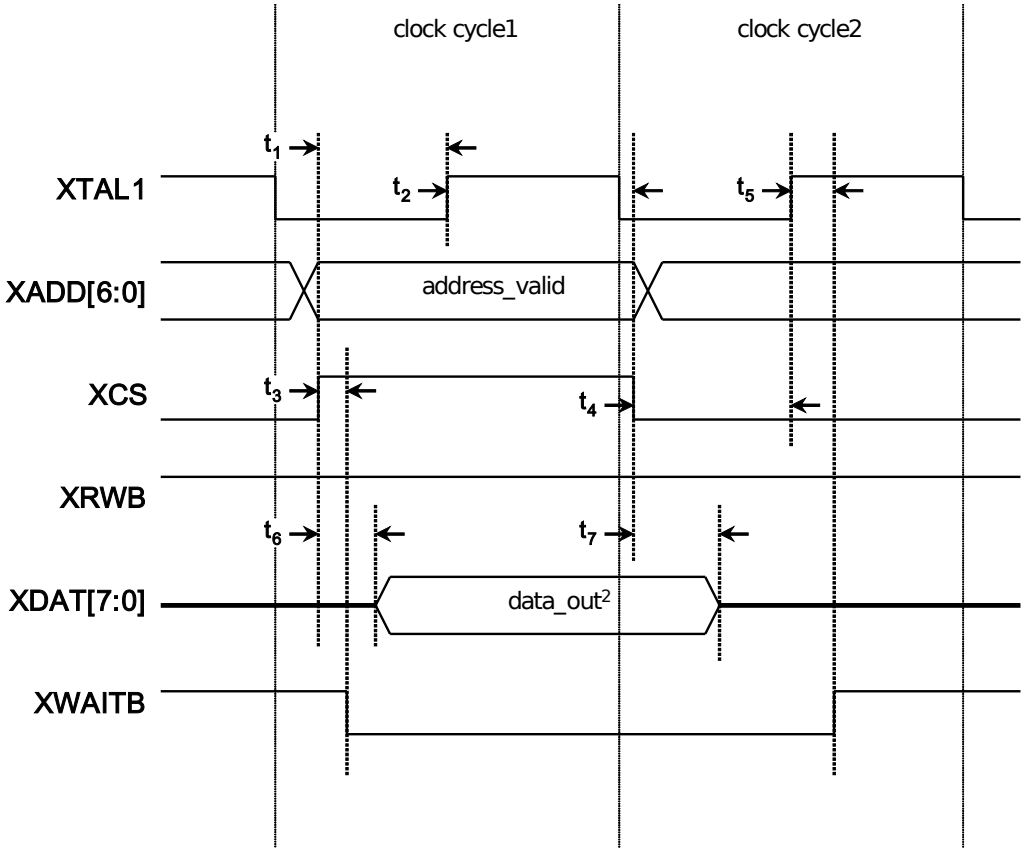
1). Write Cycle Timing



Note 1: XDAT bus driven by microcontroller

External Bus Interface Timing (cont.)

2). Read Cycle Timing



Note 2: XDAT bus driven by INT21390

External Bus Interface Timing (cont.)

(Units shown in nsec)

Name	Description	Min	Typ	Max
t_1	XADD, XCS, XRWB, XDAT valid to XTAL1 rising (data setup time, clock cycle1)	15		
t_2	XTAL1 rising to XADD, XCS, XRWB, XDAT invalid (data hold time, clock cycle1)	33		
t_3	XCS rising to XWAITB falling (clock cycle1)			5
t_4	XCS falling to XTAL1 rising (clock cycle 2)	15		
t_5	XTAL1 rising to XWAITB rising (clock cycle2)			5
t_6	XADD, XCS valid to XDAT output valid (clock cycle1)			12
t_7	XADD, XCS invalid to XDAT output invalid (clock cycle2)			12

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