INT2096

A P A C H E

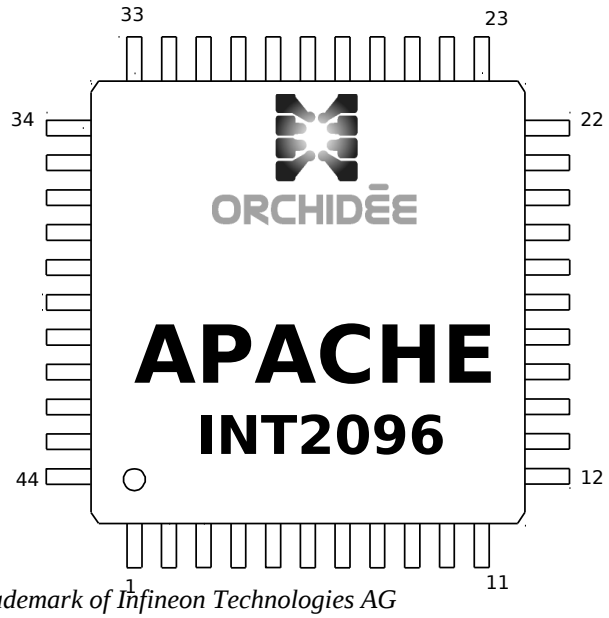
Orchidée Semiconductor 8-port NT-mode U_{pn} Line Transceiver

Features

- Pin-for-Pin replacement for industry-standard PEB2096 (OCTAT-P™) component
- Up to 3.0km (0.5mm) line interface performance (no dead zones)
- Monitor Channel register programming
- JTAG Boundary Scan support
- Single 5.0V supply
- Low Power 0.5µ technology
- 44-pin JDEC standard MQFP (Pb-free, green) package

Description

The Orchidée Semiconductor INT2096 is a fully featured replacement for the industry standard OCTAT-P™ 8-port Upn Transceiver. The chip supports loop lengths up to 3.0km over 0.5mm cable and provides all signal conditioning, equalization and adaptive threshold adjustment to optimize line performance. All other features and timing of the OCTAT-P™ are supported.



OCTAT-P is a registered trademark of Infineon Technologies AG

September, 2005

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (V_{SS} = 0V, T_J = 25^{0}C)

Parameter	Symbol	Rated Values	Unit
Power Supply Voltage	V_{DD}	-0.3 to +7.0	V
Input Voltage	V_I	-0.3 to +7.0	
Output Voltage	V_O	-0.3 to VDD	
Input Current	I_I	-10 to +10	mA
Output Current per I/O	I_O	-10 to +10	
Storage Temperature	T_{STG}	-65 to +150	^{0}C

Recommended Operating Conditions (V_{SS} = 0V)

Parameter	Symbol	Rated Values	Unit
Power Supply Voltage	V_{DD}	+4.75 to +5.25	V
Junction Temperature	T_J	-40 to +100	^{0}C

DC Characteristics (Over Operating Range)

Parameter	Symbol	Conditions	Rated Values			Unit
			Min.	Typ.	Max.	
High Level Input Voltage	V_{IH}		2.0	-	V_{DD}	V
Low Level Input Voltage	V_{IL}		0.0	-	0.8	
High Level Output Voltage	V_{OH}	I_{OH} = TBD	2.4	-	-	
Low Level Output Voltage	V_{OL}	I_{OL} = TBD	-	-	0.4	
High Level Input Current	I_I	$V_{IH} = V_{DD}$	-	-	10	uA
Low Level Input Current	I_O	$V_{IL} = V_{SS}$	-10	-	-	
3-State Output Leakage Current	I_{OZH}		-10	-	10	
	I_{OZL}		-10	-	10	
Stand-by Current	I_{DDQ}	$V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$		TBD		

Pin Descriptions

Pin	Signal	Type	Description
1	LI4A	Analog	Upn line interface
2	LI4B	Analog	Upn line interface
3	VSS	Supply	
4	LI5A	Analog	Upn line interface
5	LI5B	Analog	Upn line interface
6	VDD	Supply	
7	LI6A	Analog	Upn line interface
8	LI6B	Analog	Upn line interface
9	VSS	Supply	
10	LI7A	Analog	Upn line interface
11	LI7B	Analog	Upn line interface
12	VDD	Supply	
13	TDO	Output	JTAG port interface
14	TDI	Input	JTAG port interface
15	TCK	Input	JTAG port interface
16	TMS	Input	JTAG port interface
17	MODE	Input	Mode selection while RST high
18	SSYNCB	Input	Upn superframe sync
19	VSS	Supply	
20	XTAL1	Input	Clock input
21	XTAL2	Output	Clock output
22	VDD	Supply	
23	LI3B	Analog	Upn line interface
24	LI3A	Analog	Upn line interface
25	VSS	Supply	
26	LI2B	Analog	Upn line interface
27	LI2A	Analog	Upn line interface
28	VDD	Supply	
29	LI1B	Analog	Upn line interface
30	LI1A	Analog	Upn line interface
31	VSS	Supply	
32	LI0B	Analog	Upn line interface
33	LI0A	Analog	Upn line interface
34	VDD	Supply	
35	CLK2	Output	7.68MHz clock output
36	CLK1	Output	15.36MHz clock output
37	VSS	Supply	
38	RST	Input	Active high reset
39	IDS	Input	IOM data clock select
40	DU	Output	IOM2 data
41	DD	Input	IOM2 data
42	DCL	Input	IOM2 clock
43	FSC	Input	IOM2 frame sync
44	VDD	Supply	

Registers (Accessed via IOM2 Monitor Channel)

Name	Address	Type	Initial Value
ID Register	0	R	0x04
GCONFIG Register	1	W	0xFF (MODE=1) 0x01 (MODE=0)
BERROR Register	1	R	0x00
UCONFIG Register	2	W	0x00 (MODE=1) 0x20 (MODE=0)
CABDEL Register	2	R	0x00
SCMODL Register	8	RW	0x55
SCMODM Register	9	RW	0x55
UALA Register	A	RW	0x31

APACHE-specific Register Descriptions

APACHE contains 3 new registers which are not supported in OCTAT-P™. These registers are accessed in the same manner as the existing registers via the IOM2 Monitor Channel. The description of these registers follow.

SCMOD Registers: Scrambler Enable/Select. Allows selective, per-port enabling/disabling and scrambler algorithm selection at the Upn line interfaces.

Register	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
SCMODM	SC7[1]	SC7[0]	SC6[1]	SC6[0]	SC5[1]	SC5[0]	SC4[1]	SC4[0]
SCMODL	SC3[1]	SC3[0]	SC2[1]	SC2[0]	SC1[1]	SC1[0]	SC0[1]	SC0[0]

SCx[1:0]
- 00: Enable V.27 scrambling
- 01/10: Enable V.27(bis) scrambling, compatible with OCTAT-P™
- 11: Disable scrambler

UALA Register: Upn Analog Latency Adjust. Allows adjustment of values read from CABDEL register. The default value is set to allow cable delay values to mirror the same values which would be read from an OCTAT-P™. The resultant value read from the CABDEL register is given by:

$$CABDEL = (\#clocks - UALA) / 2$$

Where #clocks is the number of 15.36MHz clocks or 7.68MHz clocks (depending on the resolution selected) from the end of the M-bit period in a transmit frame to the beginning of the F-bit in the received frame.

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September, 2005